INTEGRATED CIRCUIT WITH MODIFIED METAL FEATURES AND METHOD OF FABRICATION THEREFOR

This application is a Divisional of U.S. Application No. 10/231,390, filed August 29, 2002, now Patent No. 6,737,346 which is incorporated herein by reference.

Technical Field

The present invention relates generally to design layout for metal layers of an integrated circuit, and more specifically to modifying the spacing between metal features that are diagonally-adjacent to one another, in order to better planarize the topology of a subsequently deposited dielectric layer over the metal features.

Background

Conventionally designed metal line layouts of integrated circuits (IC) structures can result in large spaces between nearest parallel, electrically isolated metal lines. These spacings are random in size and have a great variety of dimensions. When an intermetal dielectric layer (IDL), such as an oxide, is deposited over the metal lines having random spacing between them, the top surface of the IDL will have a highest altitude equal to the thickness of the metal features (T_{met}) plus the thickness of the IDL (T_{IDL}). In those areas where there are no metal features but only open space, the altitude of the top surface of the IDL will be T_{IDL}.

Figure 1 illustrates a side, cross-sectional view of a conventional integrated circuit structure, which includes a series of metal features 102 and an IDL 104 situated on a substrate 106. For example purposes, each metal line has a thickness, T_{met} 110, and a width, W_{met} 112. The thickness of IDL, T_{IDL}, is indicated at 114. The highest altitude of the top surface of IDL 104 is $T_{met} + T_{IDL}$, as indicated at 116.

Figure 1 shows IDL 104 as being non-planarized and having both wide 132 and narrow trenches 130 in the top surface of IDL 104. Where the spacing between two